NØAX

HANDS-ON RADIO

Experiment #77 — Load Lines

Once past the very basic levels of transistor amplifier circuits, you'll encounter the *load line*, a graphical method of circuit design. This experiment shows you how the load line is determined and applied to circuit behavior.

Diode Load Line

A diode is the simplest semiconductor device for which a load line can be drawn. Figure 1(A) shows a diode in series with a resistor load, R_L. For any given combination of V_S and R_L, if we know the diode's forward voltage, V_F, we can solve for the diode current, $I_F = (V_S - V_F) / R_L$. V_F, however, depends on I_F, so we must solve the exponential equation for I_F as a function of V_F, shown as the diode's *characteristic I-V* curve in Figure 1(B).[1]

Figure 1(B) also shows the less precise, but easier to use, graphical method of load lines. The load line describes what happens to voltage and current in R_L. It is drawn between the maximum and minimum possible values of current and voltage across R_L. For example, if $I_F = 0$, there is no voltage drop across the diode and the voltage across R_L is V_S — that's point A on the load line. Similarly, if $V_F = 0$, then $I_F = V_S/R_L$ and that's point B on the load line.

The only point at which the load line intersects the curve is point C — the *operating point* for the circuit. The intersection is the solution of the diode's characteristic curve equation with the known value of R_L and V_S. If either V_S or R_L change, the slope or placement of the load line will change along with its intersection with the diode's characteristic curve. Let's try it!

[1]The Fundamental Diode Equation is presented in the "Analog Basics" chapter of any recent *ARRL Handbook*.

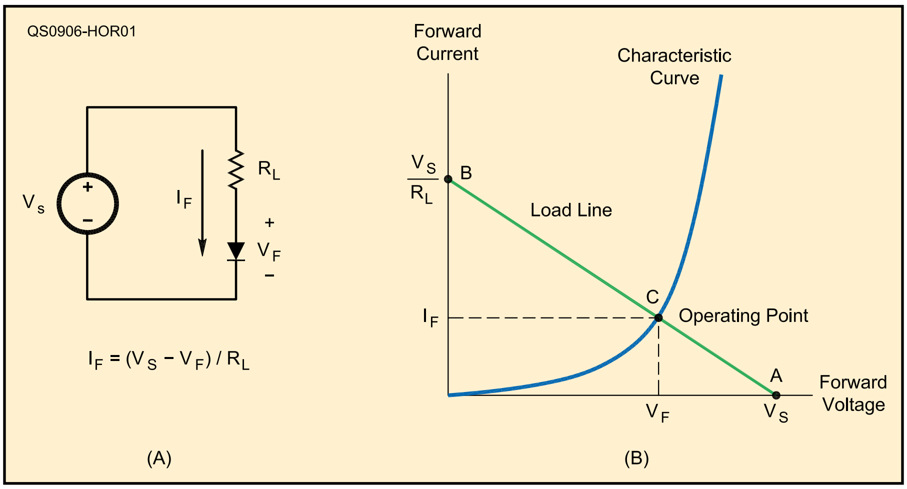

Figure 1 — The simple circuit at (A) can be used to determine the diode's characteristic curve at (B). The intersection of the load line and the characteristic curve is the circuit's operating point.

Operating Point Control

Build the circuit in Figure 1(A) using a 1N4001 silicon diode rectifier, $V_S = 3$ V, and $R_L = 1$ kΩ. Prepare a graph with the I_F axis showing 0 to 50 mA and the V_F axis showing 0 to 10 V. Draw the load line between point A ($I_F = 0$ mA, $V_F = V_S = 3$ V) and point B ($I_F = V_S / R_L = 3$ mA, $V_F = 0$ V).

Measure the diode's forward voltage, V_F, and use Ohm's Law to calculate I_F from the voltage across R_L or measure it directly with a meter. The values should be somewhere around 0.6 V and 2.4 mA. When that point is plotted, it should be very close to or on the load line.

Vary V_S from 1 to 10 V in steps of 1 V, calculating point A and B and drawing a new load line at each step. Measure the diode voltage and circuit current as before, plotting the combination on the graph and confirming that each point is on a load line. You will start to see the diode's characteristic curve appear as the sequence of plotted points!

Return V_S to 3 V and change R_L to each of the following values, drawing a new load line at each step: 100, 220, 470, 1000, 2.2 k, and 4.7 kΩ. Measure and plot V_F and I_F at each step. This will fill in even more points, each very close to the load line for that value of R_L. As you can see, if you had enough values of R_L and sufficient power supply range, you could determine the diode's characteristic curve exactly!

You'll also have noticed that while you were only varying V_S, the load lines were parallel, but when R_L was varied, the load line slopes changed. That's because the slope of the load line is $-1/R_L$. Lower load resistance results in a steeper load line.

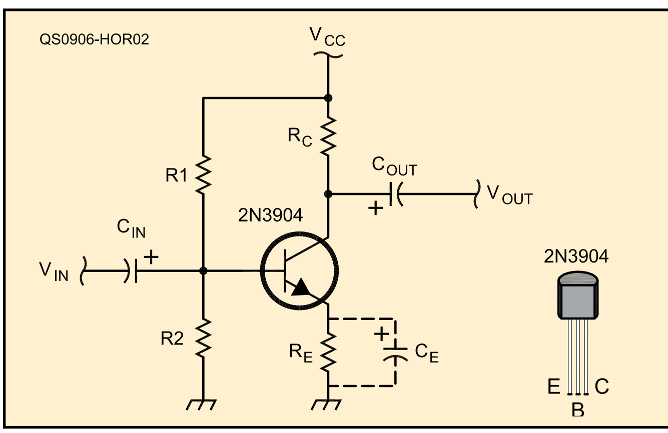

Figure 2 — The common-emitter (CE) amplifier uses a resistive voltage divider (R1 and R2) to establish the circuit's Q point along with R_E. The capacitor C_E is an emitter bypass capacitor that provides higher ac gain while leaving dc biasing unaffected.

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Transistor Amplifier Load Line

The load line is much more useful in designing transistor circuits, since current and voltage can take wide ranges of values. The common emitter (CE) amplifier in Figure 2, from the first Hands-On Radio experiment is one you'll use frequently, so we'll use it as an example.[2] This circuit uses self bias and emitter degeneration to establish a stable *Q point* (the operating point with no input signal).

The characteristic curves for a typical 2N3904 NPN transistor in the CE configuration are shown in Figure 3. Instead of just having a single characteristic curve as did the diode, a transistor's I_C–V_{CE} characteristic curve can change. As base current varies, the height of the curve changes on the graph. The set of curves show "snapshots" of the transistor's characteristic curve, each at a different value of base current.

Because the load for the circuit is resistive (consisting of R_C+R_E), the operating point falls along the dc load line drawn on the characteristic curves. We'll get to the ac load line later. As with the diode circuit, the intersection of the load line with the characteristic curve corresponding to the value of base current is the circuit's operating point. If you imagine one of the constant base current lines moving up and down as an input signal varies the base current, you can see its intersection with the load line moving, too. When no signal is applied, the base current is fixed at the level of bias current chosen by the designer and that operating point is the circuit's Q point. In the case of our CE amplifier, the values of R_1, R_2 and R_E determine the location of the Q point by controlling the value of the base bias current.

V_{CC} and the values of R_C and R_E determine the orientation of the load line. The two end points of the load line correspond to transistor saturation [$I_{Csat} = V_{CC} / (R_C+R_E)$ on the I_C axis] and cutoff (V_{CC} on the V_{CE} axis). The slope of the load line is $-1/(R_C+R_E)$, because the output current of the transistor flows through both the collector and emitter resistors.

In order to experiment with the load line, here are a set of components that will result in a Q point of I_{CQ} = 4 mA, V_{CEQ} = 5 V and a voltage gain of –5 with V_{CC} = +12 V: R_E = 270 Ω, R1 = 39 kΩ, R2 = 6.8 kΩ, and RC = 1.5 kΩ. (10 μF capacitors will be fine for C_{IN} and C_{OUT}.) Download and print the sample 2N3904 characteristic curves from the Hands-On Radio Web site and draw the load line between cutoff and saturation in this circuit. (The Q point should be on the load line.)

Build the circuit and verify that the values of I_{CQ} and V_{CEQ} are about right. Apply a 1 kHz, 0.5 V_{P-P} sine wave at the input and verify that the output signal is about five times larger and inverted from the input. Increase the input voltage until the output waveform becomes clipped at either the top or bottom and then reduce the input voltage by about half.

Now move the Q point by changing the value of I_{BQ}. To do this without changing the load line, adjust the ratio of R1 and R2 to change V_B, keeping the sum of the resistors in the range of 20 k to 50 kΩ. (You can substitute a 50 kΩ potentiometer for R1 and R2, with the wiper connected to the transistor base.) Measure the new values of I_{CQ} and V_{CEQ}, locate the new Q point on the load line, and observe the effect on the output waveform. For example, doubling the value of R2 will raise the value of I_{BQ} dramatically and probably cause the output waveform to be clipped at the bottom. This is because the higher bias current has moved the Q point farther along the load line toward saturation (left), making it easier for an input signal to drive V_{CE} lower into the saturation region.

[2]Previous Hands-On Radio columns and a complete parts list for all experiments are available to ARRL members at **www.arrl.org/tis/info/HTML/Hands-On-Radio** and in Experiment #76 (see next note).

AC Load Lines

Figure 2 shows an *emitter bypass* capacitor, C_E, next to R_E. When C_E is connected across R_E, the circuit has a different ac voltage gain $A_V = -R_C/r_e$ (r_e is the internal emitter resistance of a few ohms) than dc gain $A_V = -R_C/R_E$. For an ac signal, the circuit operates on a separate ac load line as shown in Figure 3, because R_E has been effectively short circuited for ac signals. Without R_E, the slope of the ac load line is $-1/R_C$, steeper than for the dc load line. The ac and dc load lines intersect at the circuit's Q point because the circuit's ac and dc operation is the same if the ac input signal is zero.

Parts List[3]

- 1N4001 diode
- 2N3904 transistor
- 100, 220, 270, 470, 1000, 1.5 k, 2.2 k, 4.7 k, 6.8 k and 39 kΩ, ¼ W resistors
- 3 each 10 μF, 25 V electrolytic capacitors

Recommended Reading

Even for non-engineers, used copies of first- and second-year circuit engineering textbooks make fine workbench references for all sorts of circuit questions. Two of my favorites are Hayt and Kemmerly's *Engineering Circuit Analysis* and Millen and Grabel's *Microelectronics*, both published by McGraw-Hill. The former is good for basic R-L-C circuit mechanics and the latter for semiconductor circuits.

Next Month

You've heard terms before such as "SWR bridge," "noise bridge," "Wheatstone bridge" and so forth. We'll cross that bridge next month as we take a look at bridge circuits and why they are so useful.

[3]A parts kit for the first 61 experiments is available from your ARRL dealer or the ARRL Bookstore, ARRL order no. 1255K. Telephone 860-594-0355, or toll-free in the US 888-277-5289; **www.arrl.org/shop/**; **pubsales@arrl.org**.

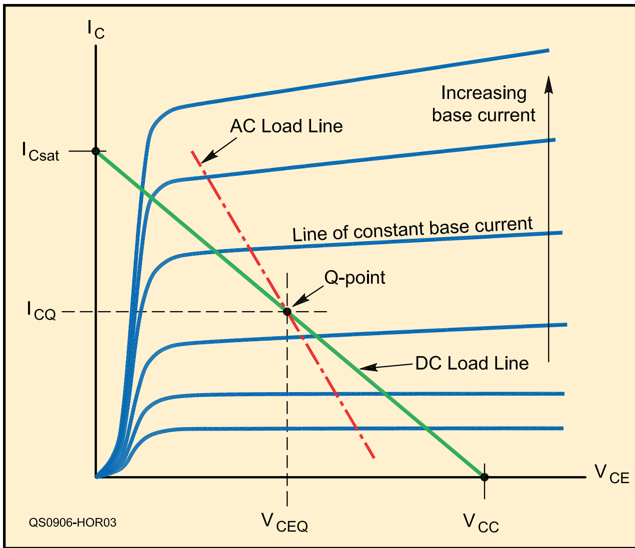

Figure 3 — The dc load line's end points correspond to transistor saturation (I_{Csat}) and cutoff (V_{CC}). The circuit operates somewhere on the load line depending on bias. The operating point with no signal applied is the quiescent, or Q point. By adding an emitter bypass capacitor, there is less load impedance for an ac signal, increasing the slope of the ac load line.

Strays

I would like to get in touch with...

◊ any Amateur Radio ops who are employed by Munich Reinsurance America Inc. — *Mike Haydon, AC2Q, 1420 Fairway, Rantoul, IL 61866, tel 217-892-1658*